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SHEET 1 OF 7

FORM PTO - 1449

SUPPLEMENTAL INFORMATION  
DISCLOSURE STATEMENT

ATTORNEY DOCKET NO.: ASC-044

APPLICANT(S): Fitzgerald et al.

SERIAL NO.: 09/884,172

FILING DATE: June 19, 2001      GROUP: 2822

## U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A46	4,010,045	3/1/1977	Ruehrwein			4/27/1976
	A47	4,997,776	3/1/1991	Haramé et al.			6/20/1990
	A48	5,013,681	5/7/1991	Godbey et al.			9/29/1989
	A49	5,166,084	11/24/1992	Pfiester			9/3/1991
	A50	5,177,583	1/1/1993	Endo et al.			1/10/1991
	A51	5,202,284	4/1/1993	Kamins et al.			12/1/1989
	A52	5,207,864	5/4/1993	Bhat et al.			12/30/1991
	A53	5,208,182	5/4/1993	Narayan et al.			11/12/1991
	A54	5,212,110	5/18/1993	Pfiester et al.			5/26/1992
	A55	5,221,413	6/22/1993	Brasen et al.			4/24/1991
	A56	5,250,445	10/1/1993	Bean et al.			1/17/1992
	A57	5,285,086	2/1/1994	Fitzgerald			6/18/1992
	A58	5,298,452	3/1/1994	Meyerson			2/21/1992
	A59	5,310,451	5/10/1994	Tejwani et al.			8/19/1993
	A60	5,346,848	9/13/1994	Gruppen-Shemansky et al.			6/1/1993
	A61	5,374,564	12/20/1994	Bruel			12/20/1994
	A62	5,399,522	3/1/1995	Ohori.			3/21/1995
	A63	5,413,679	5/9/1995	Godbey et al.			6/30/1993
	A64	5,426,069	6/20/1995	Selvakumar et al.			4/9/1992
	A65	5,461,243	10/24/1995	Ek et al.			10/29/1993
	A66	5,462,883	10/31/1995	Dennard et al.			4/11/1994
	A67	5,476,813	12/19/1995	Naruse			11/14/1994
	A68	5,484,664	1/16/1996	Kitahara et al.			1/21/1994
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	A69	5,536,361	7/16/1996	Kondo et al.			1/23/1995
	A70	5,540,785	7/30/1996	Dennard et al.			4/4/1994
	A71	5,630,905	5/1/1997	Lynch et al.			6/5/1995
	A72	5,659,187	8/1/1997	Legoues et al.			6/7/1995
	A73	5,714,777	2/3/1998	Ismail et al.			2/19/1997
	A74	5,728,623	3/17/1998	Mori			3/16/1995
	A75	5,759,898	6/2/1998	Ek et al.			12/19/1996
	A76	5,786,612	7/28/1998	Otani et al.			4/16/1996
	A77	5,877,070	3/2/1999	Goesele et al.			5/31/1997
	A78	5,906,708	5/25/1999	Robinson et al.			12/6/1995
	A79	5,943,560	8/24/1999	Chang et al.			4/19/1996
	A80	5,966,622	10/12/1999	Levine et al.			10/8/1997
	A81	6,033,974	3/7/2000	Henley et al.			8/10/1999
	A82	6,033,995	3/7/2000	Muller			9/16/1997
	A83	6,074,919	6/13/2000	Gardner et al.			1/20/1999
	A84	6,103,559	8/15/2000	Gardner et al.			3/30/1999
	A85	6,133,799	10/17/2000	Favors, Jr., et al.			2/25/1999
	A86	6,140,687	10/31/2000	Shimomura et al.			11/26/1997
	A87	6,153,495	11/28/2000	Kub et al.			3/9/1998
	A88	6,154,475	11/28/2000	Soref et al.			12/4/1997
	A89	6,160,303	12/12/2000	Fattaruso			8/26/1998
	A90	6,162,688	12/19/2000	Gardner et al.			1/14/1999
	A91	6,184,111	2/6/2001	Henley et al.			8/10/1999
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	A92	6,191,007	2/20/2001	Matsui et al.			4/28/1998
	A93	6,191,432	2/20/2001	Sugiyama et al.			9/2/1997
	A94	6,194,722	2/27/2001	Fiorini et al.			3/27/1998
	A95	6,210,988	4/3/2001	Howe et al.			1/14/2000
	A96	6,218,677	4/17/2001	Broekaert			8/15/1994
	A97	6,232,138	5/15/2001	Fitzgerald et al.			11/24/1998
	A98	6,235,567	5/22/2001	Huang			8/31/1999
	A99	6,261,929	7/1/2001	Gehrke et al.			2/24/2000
	A100	6,271,551	8/7/2001	Schmitz et al.			12/13/1996
	A101	6,271,726	8/7/2001	Fransis et al.			1/10/2000
	A102	6,313,016	11/6/2001	Kibbel et al.			12/22/1999
	A103	6,323,108	11/27/2001	Kub et al.			7/27/1999
	A104	6,329,063	12/11/2001	Lo et al.			12/11/1998
	A105	6,335,546	1/1/2002	Tsuda et al.			7/30/1998
	A106	6,368,733	4/9/2002	Nishinaga, Tatau			8/5/1999
	A107	6,372,356	4/16/2002	Thornton et al.			4/28/2000
	A108	6,403,975	6/11/2002	Brunner et al.			04/08/1997
	A109	6,425,951	7/30/2002	Chu et al.			8/6/1999
	A110	6,429,061	8/6/2002	Rim			7/26/2000
	A111	6,521,041	2/18/2003	Wu et al.			4/9/1999
	A112	2001/0003269	6/14/2001	Wu et al.			4/9/1999
	A113	2002/0140031	10/3/2002	Rim			3/31/2001
	A114	2002/0024395	02/28/2002	Akatsuka et al.			6/14/2001
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EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE		
	A115	2002/0043660	04/18/2002	Yamazaki et al.					
	A116	2002/0052084	05/02/2002	Fitzgerald			5/16/2001		
	A117	2002/0068393	6/6/2002	Fitzgerald et al.			8/6/2001		
	A118	2002/0072130	6/13/2002	Cheng et al.			8/10/2001		
	A119	2002/0096717	7/25/2002	Chu et al.			1/25/2001		
	A120	2002/0100942	8/1/2002	Fitzgerald et al.			6/19/2001		
	A121	2002/0123167	9/5/2002	Fitzgerald			7/16/2001		
	A122	2002/0123183	9/5/2002	Fitzgerald			7/16/2001		
	A123	2002/0123197	9/5/2002	Fitzgerald et al.			6/19/2001		
	A124	2002/0125471	9/12/2002	Fitzgerald et al.			12/4/2001		
	A125	2002/0125497	7/16/2002	Fitzgerald			7/16/2001		
	A126	2002/0168864	11/14/2002	Cheng et al.			4/4/2002		
	A127	2003/0003679	1/2/2003	Doyle et al.					
	A128	2003/0013323	01/16/2003	Hammond et al.			6/14/2002		
	A129	2003/0025131	02/06/2003	Lee et al.			8/2/2002		
	A130	2003/0057439	03/27/2003	Fitzgerald			8/9/2002		
<b>FOREIGN PATENT DOCUMENTS</b>									
EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B25	0 514 018	11/19/1992	EP				NO	YES
	B26	0 587 520	3/16/1994	EP				NO	YES
	B27	0 828 296	3/11/1998	EP				NO	YES
	B28	00/48239	8/17/2000	WO				NO	YES
	B29	01/22482	3/29/2001	WO				NO	YES
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	B30	02/082514	10/17/2002	WO				NO	YES
	B31	02/27783	4/4/2002	WO				NO	YES
	B32	2 342 777	4/19/2000	GB				YES	YES
	B33	2 701 599	9/1/1993	FR				YES	YES
	B34	2000-031491	1/28/2000	JP				NO	NO
	B35	2002-076334	3/15/2002	JP				NO	YES
	B36	2002-164520	6/7/2002	JP				NO	YES
	B37	2002-289533	10/4/2002	JP				NO	YES
	B38	5-166724	07/23/1993	JP				NO	Abstract only
	B39	6-177046	06/24/1994	JP				NO	Abstract only
	B40	6-244112	09/02/1994	JP					
	B41	6-252046	09/09/1994	JP				NO	Abstract only
	B42	7-094420	04/07/1995	JP				NO	Abstract only
	B43	7-240372	09/12/1995	JP				NO	Abstract only
OTHER ART, JOURNAL ARTICLES, ETC.									
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)								
	C48	Armstrong, "Technology for SiGe Heterostructure-Based CMOS Devices", PhD Thesis, Massachusetts Institute of Technology, 1999, pp. 1-126.							
	C49	Augusto et al., "Proposal for a New Process Flow for the Fabrication of Silicon-based Complementary MOD-MOSFETs without ion Implantation," Thin Solid Films, vol. 294, no. 1-2, pp. 254-258 (February 15, 1997).							
	C50	Barradas et al., "RBS analysis of MBE-grown SiGe/(001) Si heterostructures with thin, high Ge content SiGe channels for HMOS transistors," Modern Physics Letters B (2001) (abstract).							
	C51	Borenstein et al., "A New Ultra-Hard Etch-Stop Layer for High Precision Micromachining," Proceedings of the 1999 12 <sup>th</sup> IEEE International Conference on Micro Electro Mechanical Systems (MEMS) (January 17-21, 1999) pp. 205-210.							
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	C52	Bruel et al., "©SMART CUT: A Promising New SOI Material Technology," Proceedings 1995 IEEE International SOI Conference (October 1995) pp. 178-179.	
	C53	Bruel, "Silicon on Insulator Material Technology," Electronic Letters, Vol. 13, No. 14 (July 6, 1995) pp. 1201-1202.	
	C54	Burghartz et al., "Microwave Inductors and Capacitors in Standard Multilevel Interconnect Silicon Technology", IEEE Transactions on Microwave Theory and Techniques, Vol. 44, No. 1, January 1996, pp. 100-104.	
	C55	Chang et al., "Selective Etching of SiGe/Si Heterostructures," Journal of the Electrochemical Society, No. 1 (January 1991) pp. 202-204.	
	C56	Feijoo et al., "Epitaxial Si-Ge Etch Stop Layers with Ethylene Diamine Pyrocatechol for Bonded and Etchback Silicon-on-Insulator," Journal of Electronic Materials, Vol. 23, No. 6 (June 1994) pp. 493-496.	
	C57	Gray and Meyer, "Analysis and Design of Analog Integrated Circuits", John Wiley & Sons, 1984, pp. 605-632.	
	C58	Huang et al., "High-quality strain-relaxed SiGe alloy grown on implanted silicon-on-insulator substrate," Applied Physics Letters, Vol. 76, No. 19 (May 8, 2000) pp. 2680-2682.	
	C59	Huang et al., "The Impact of Scaling Down to Deep Submicron on CMOS RF Circuits", IEEE Journal of Solid-State Circuits, Vol. 33, No. 7, July, 1998, pp. 1023-1036.	
	C60	IBM Technical Disclosure Bulletin, Vol. 35, No. 4B (September 1992), "2 Bit/Cell EEPROM Cell Using Band to Band Tunneling for Data Read-Out," pp. 136-140.	
	C61	IBM Technical Disclosure Bulletin, Volume 32, No. 8A, January 1990, "Optimal Growth Technique and Structure for Strain Relaxation of Si-Ge Layers on Si Substrates", pp. 330-331.	
	C62	Ishikawa et al., "Creation of Si-Ge-based SIMOX structures by low energy oxygen implantation," Proceedings 1997 IEEE International SOI Conference (October 1997) pp. 16-17.	
	C63	Ishikawa et al., "SiGe-on-insulator substrate using SiGe alloy grown Si(001)," Applied Physics Letters, Vol. 75, No. 7 (August 16, 1999) pp. 983-985.	
	C64	Ismail, "Si/SiGe High-Speed Field-Effect Transistors," Electron Devices Meeting, Washington, D.C. (December 10, 1995) pp. 20.1.1-20.1.4.	
	C65	Kim et al., "A Fully Integrated 1.9-GHz CMOS Low-Noise Amplifier", IEEE Microwave and Guided Wave Letters, Vol. 8, No. 8, August 1998, pp. 293-295.	
	C66	Kuznetsov et al., "Technology for high-performance n-channel SiGe modulation-doped field-effect transistors," J. Vac. Sci. Technol., B 13(6), pp. 2892-2896 (November/December 1995).	
	C67	Larson, "Integrated Circuit Technology Options for RFIC's□Present Status and Future Directions", IEEE Journal of Solid-State Circuits, Vol. 33, No. 3, March 1998, pp. 387-399.	
	C68	Lee and Wong, "CMOS RF Integrated Circuits at 5 GHz and Beyond", Proceedings of the IEEE, Vol. 88, No. 10, October 2000, pp. 1560-1571.	
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	C69	Lu et al., "High Performance 0.1 $\mu$ m Gate-Length P-Type SiGe MODFET's and MOS-MODFET's", IEEE Transactions on Electron Devices, Vol. 47, No. 8, August 2000, pp. 1645-1652.	
	C70	M. Kummer et al., "Low energy plasma enhanced chemical vapor deposition," Materials Science and Engineering B89 (2002) pp. 288-295.	
	C71	Maszara, "Silicon-On-Insulator by Wafer Bonding: A Review," Journal of the Electrochemical Society, No. 1 (January 1991) pp. 341-347.	
	C72	Mizuno et al., "Electron and Hole Mobility Enhancement in Strained-Si MOSFET's on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," IEEE Electron Device Letters, Vol. 21, No. 5 (May 2000) pp. 230-232.	
	C73	Mizuno et al., "High Performance Strained-Si p-MOSFETs on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," IEEE IEDM Technical Digest, (1999 International Electron Device Meeting) pp. 934-936.	
	C74	Nayak et al., "High-Mobility Strained-Si PMOSFET's"; IEEE Transactions on Electron Devices, Vol. 43, No. 10, October 1996, pp. 1709-1716.	
	C75	Papananos, "Radio-Frequency Microelectronic Circuits for Telecommunication Applications", Kluwer Academic Publishers, 1999, pp. 115-117, 188-193.	
	C76	Rim et al., "Enhanced Hole Mobilities in Surface-channel Strained-Si p-MOSFETs"; IEDM, 1995, pp. 517-520.	
	C77	Rim et al., "Fabrication and Analysis of Deep Submicron Strained-Si N-MOSFET's"; IEEE Transactions on Electron Devices, Vol. 47, No. 7, July 2000, pp. 1406-1415.	
	C78	Rim, "Application of Silicon-Based Heterostructures to Enhanced Mobility Metal-Oxide-Semiconductor Field-Effect Transistors", PhD Thesis, Stanford University, 1999; pp. 1-184.	
	C79	Sadek et al., "Design of Si/SiGe Heterojunction Complementary Metal-Oxide-Semiconductor Transistors," IEEE Trans. Electron Devices (August 1996) pp. 1224-1232.	
	C80	Sugimoto and Ueno, "A 2V, 500 MHz and 3V, 920 MHz Low-Power Current-Mode 0.6 $\mu$ m CMOS VCO Circuit", IEICE Trans. Electron., Vol.E82-C, No. 7, July 1999, pp. 1327-1329.	
	C81	Ternent et al., "Metal Gate Strained Silicon MOSFETs for Microwave Integrated Circuits", IEEE October 2000, pp. 38-43.	
	C82	Welser et al., "Electron Mobility Enhancement in Strained-Si N-Type Metal-Oxide-Semiconductor Field-Effect Transistors," IEEE Electron Device Letters, Vol. 15, No. 3 (March 1994) pp. 100-102.	
	C83	Welser, "The Application of Strained Silicon/Relaxed Silicon Germanium Heterostructures to Metal-Oxide-Semiconductor Field-Effect Transistors," PhD Thesis, Stanford University, 1994, pp. 1-205.	
	C84	Wolf and Tauber, Silicon Processing for the VLSI Era, Vol. 1: Process Technology, Lattice Press, Sunset Beach, CA, pp. 384-386 (1986).	
	C85	Yeo et al., "Nanoscale Ultra-Thin-Body Silicon-on-Insulator P-MOSFET with a SiGe/Si Heterostructure Channel," IEEE Electron Device Letters, Vol. 21, No. 4 (April 2000) pp. 161-163.	
	C86	Zhang et al., "Demonstration of a GaAs-Based Compliant Substrate Using Wafer Bonding and Substrate Removal Techniques," Electronic Materials and Processing Research Laboratory, Department of Electrical Engineering, University Park, PA 16802 (1998) pp. 25-28.	
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